Developing New Methods To Find The Number Of RAM Chips In The Memory Decoding To Construct The Required Memory Size

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1. Abstract

Integrated –Circuit random access memory RAM chips are available in a variety of sizes. If the memory unit needed for an application is larger than the size of one chip, it is necessary to construct an array of RAM chips which includes a combined number of RAM chips. The problem here is how to determine the dimensions of the array of RAM chips. This paper develops new methods to find the number of RAM chips in the array of RAMS in order to obtain the required memory size.

2. Introduction

A memory unit is a collection of storage cells together with associated circuits needed to transfer information in and out of the device. Memory cells can be accessed for information transfer to or from any desired random location , so the name random-access memory, defined as RAM [1].

A memory unit stores the binary information in words, these words are groups of bits. Each word is an entity of bits that move in and out of storage as a unit.[5],[1].

The communication between a memory and its environment is achieved through data input and output lines, address selection lines, and control lines that specify the direction of transfer. All of these elements are shown in the following figure[5],[6]**:**

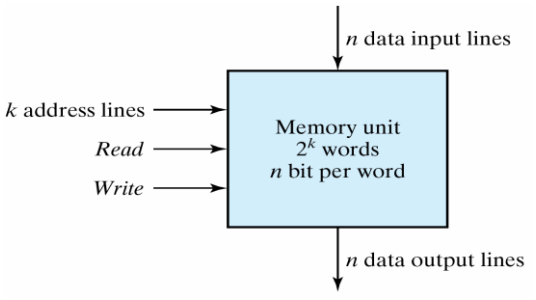

Figure 1 : Block Diagram of a memory unit

According to figure: 1, If there is a (2k * 4) RAM, this means:

(2k * 4) RAM = (2*2^10 * 4) = (2^11 * 4) RAM and from this we can conclude:

- The number of address lines = 11
- The number of words = 2^11
- The number of bits per word = 4

This research focuses on the communication between memory units in order to obtain a large memory size from small size memories .This is known and applicable by memory decoding winch includes an array of small size RAM chips to provide a large size of RAM., The new something that paper shows is how to determine the size of array of ram chips directly by knowing the size of small Ram and the wanted large size, It implements a mathematical equations that provide the following:

a- The number of rows in the array of Ram chips.
b- The number of columns in the array of Ram chips.
c- Also, the total number of Ram chips.
d- The type of the decoder used in the memory decoding.
e- The number of external logic OR – gates in the memory decoding.

3. Making Larger Memories

By using the CS lines, we can make larger memories from smaller ones by tying all address, data, and R/W lines in parallel, and using the decoded higher order address bits to control CS. Using the 4-Word by 1-Bit memory from before, we can construct a 16-Word by1-Bit memory. See the following figure [5],[6]:

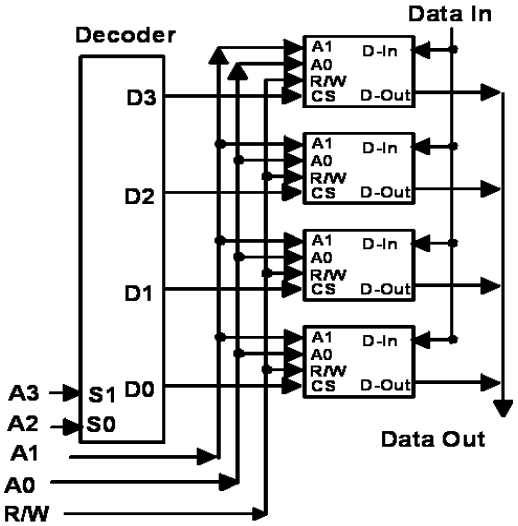

Figure 2 : Block Diagram of making a large memory

3.1 Making Wider Memories

To construct wider memories from narrow ones, we tie the address and control lines in parallel and keep the data lines separate. For example, to make a 4-word by 4-bit memory from 4, 4-word by 1-bit memories. Note that both 16x1 and 4x4 memories take 4-chips and hold 16 bits of data. See the following figure[5],[6]:

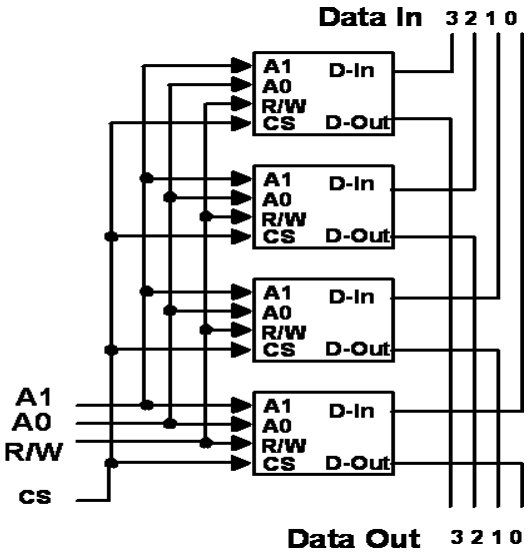

Figure 3 : Block Diagram of making a wider memory

3.2 The developed methods to find the number of RAM chips in the array of RAMS in order to obtain the required memory size

The methods of this research suppose the size of big Ram as :

X_1 U * N_1 RAM……..…(1)

And also suppose the size of small Ram as :

X_2 U * N_2 RAM…….…...(2)

Where:

X: is an integer number.
U: The unit of the size (ex: K: Kilo, M :Mega, G : Giga,..)
N: The number of bits in each word.

The number of rows in the array of RAM chips will be (R)

$R = X_1 / X_2$……..(3)

.

The number of columns in the array of RAM chips will be (C)

$C = N_1 / N_2$…..…….…..**.....**(4)

The total number of small RAM needed will be calculated by The following equation:

R * C ……..…..(5)

3.3 Using The Research Methods in Application Example

Suppose you need a memory array with 16k × 8 organization, but all you have on hand are 4k × 8 memory chips. How many 4k* 8 Ram chip needs ?

The size of big RAM is 16k * 16, By applying eqn (1) we obtain:

$X_1 = 16$ and $N_1 = 16$

The size of small RAM is 4k * 8, By applying eqn (2) we obtain

$X_2 = 4$ and $N_2 = 8$

Now :

The number of rows in the array of RAM chips

$$R = X_1 / X_2 \text{ , from eqn (3)}$$

$$R = 16 / 4 = 4 \text{ Rows}$$

The number of columns in the array of RAM chips

$$C = N_1 / N_2 \text{ , from eqn (4)}$$

$$C = 16 / 8 = 2 \text{ Columns}$$

The total number of small RAM chips needed

$$= R * C \text{ , from eqn (5)}$$

$$= 4 * 2 = 8 \text{ chips from (4k * 8) RAM.}$$

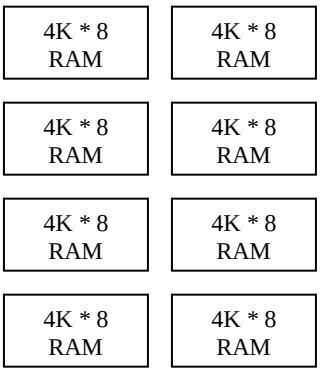

Figure 4 : Block Diagram of multiple 4K * 8 RAM

3.4 How to build a memory array from multiple Smaller RAMs to obtain Larger RAMs:

Here there is a necessary to find the suitable decoder, and also the number of external logic OR gates, the research methods in section 3.2 achieve these requirements.

From equation (3), R can help us to find the decoder type, Since the value of R here means the output of the decoder which equals 2 ^n , so we can determine the type of decoder which is (n * 2^n).

The number of OR gates can be obtained from equation (2), C here refers to the number of OR gates needed.

3.4.a Application Example

Suppose you need a memory array with 8k × 16 organization, but all you have on hand are 2k × 4 memory chips. How many 2k* 4 Ram chip needs ? Show how you could connect them to form the desired array ?

The size of big RAM is 8k * 16, By applying eqn (1) we obtain:

$$X_1 = 8 \quad \text{and} \quad N_1 = 16$$

The size of small RAM is 2k * 4, By applying eqn (2) we obtain

$$X_2 = 2 \quad \text{and} \quad N_2 = 4$$

Now:
The number of rows in the array of RAM chips (R)

$$R = X_1 / X_2 \text{ , from eqn (3)}$$

$$R = 8 / 2 = 4 \text{ Rows}$$

The number of columns in the array of RAM chips (C)

$$C = N_1 / N_2 \text{ , from eqn (4)}$$

$$C = 16 / 4 = 4 \text{ Columns}$$

The total number of small RAM chips needed

$$= R * C \text{ , from eqn (5)}$$

$$= 4 * 4 = 16 \text{ chips from (2k * 4) RAM}$$

We can determine the decoder type from the value of R , eqn(3), the R equals 4, so the output of the decoder 2^n = 4 , and this implies that the input of the decoder is n = 2, this means that the decoder type is (2 * 4) decoder.

Also, we can determine the number of OR gates needed from the value of C eqn(4), so the number of OR gates = C = 4 OR gates.

From the previous analysis by using the research methods, we can draw the following block diagram of a 8k * 16 RAM :

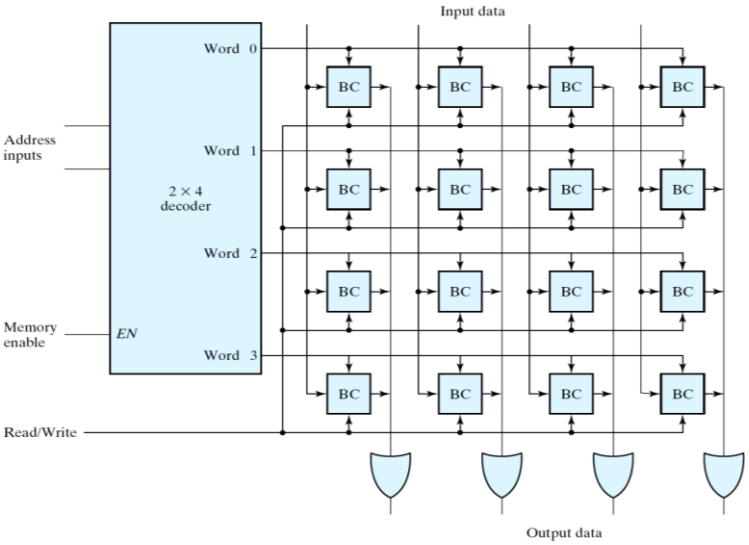

Figure 5: Block diagram of a 8k * 16 RAM

4.Conclusion

The constructing a big RAM size from multiple small RAM size is very important in memory organization, especially if there is only a small RAM size, and there is a need to a big size. The memory decoding solves this problem by constructing an array of RAM chips, which includes a combined number of small size RAMS to form the required memory size. This paper implements mathematical equations in order to determine the dimensions of the array of RAM chips, these equations provide the number of rows and columns in the array and also the total number of small RAM chips needed. On the other hand these equations may be used to determine the suitable decoder type and the number of OR logic gates which are used in the building of the array of small RAM chips.

References

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